Operating System Policies for Improved Reliability on MPSoCs

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Project Description

With the growing complexity in consumer embedded products, a new-born generation of System-on-Chip (SoC) architectures consisting of complex integrated components communicating with each other at very high-speed rates is being envisioned. One of their main design challenges will be the prototyping and power optimization of SoCs consisting of hundreds of processing cores (Multi-ProcessingSoC or MPSoC), with high power density and thermal issues. One of the main effects of the thermal increase is the premature aging of the CMOS devices, reducing the mean-time-to-failure (MTTF) metric. Therefore, there is a need for the development of techniques and policies that improve the reliability of these multi-processor systems.

During the last years, several approaches have been proposed to deal with the premature aging of the CMOS devices. Many of them propose the use of extra hardware that provides the required redundancy in case of failure. Others make more complex the integrated logic in order to prevent those mechanisms that speed up the aging of the CMOS devices. However, these techniques increase the complexity of the hardware, generate an area and power overhead, and many times impact on the system performance.

Most of these multi-processor systems count with hardware modules that tune the working frequency and voltage of the cores to reduce the power consumption (Frequency and Voltage Scaling). These modules can be controlled by dynamic hardware approaches or, usually, by the Operating System (OS). The OS can select the voltage and frequency setup of the processor according to their workload and attending to power, thermal or, in this case, reliability constraints. Also, in the case of heterogeneous MPSoCs where there are different processing cores, the OS can select the assignment of the tasks to balance the workload or reduce the premature aging of the devices.

The goals of this project are, on one hand, to study the effect of the OS task and hardware management on the reliability of the system. On the other hand, after the analysis stage, several policies that improve the MTTF of the system will be envisioned and implemented. This work will be conducted with an FPGA-based implementation of a multi-processor system in a Virtex 2 board. The system runs a modified release of uClinux OS and the proposed policies will be implemented in it. The emulation platform also provides the required information to analyze the reliability of the MPSoC.

Tasks of the Student

The tasks expected by the student developing this project are very briefly described in the following:

- Study of the voltage and frequency scaling (VS/FS) mechanisms existing in the FPGA-based multi-processor system.
- Study of the task assignment and VS/FS policies implemented in uClinux and their impact on the system reliability.
- Development of several OS policies that improve the system reliability by the tuning of the hardware and software resources.

Requirements

This project involves knowledge of various aspects of digital system designs, namely:

- Advanced knowledge of C/C++ programming languages, and SoC architectures.
- Advanced knowledge of Operating Systems, schedulers and task assignment mechanisms.

Key words

MPSoC, System-on-Chip, FPGA, reliability, Operating System, scheduling.